ABSTRACT OF THE DISCLOSURE

A semiconductor integrated circuit for decreasing level fluctuation in an output signal of a level conversion circuit. The level conversion circuit has a pair of series-connected transistors including a first MOS transistor and a second MOS transistor and a further pair of series-connected transistors including a third MOS transistor and a fourth MOS transistor. The level conversion circuit generates a first output signal from a node connecting the first and second MOS transistors and a second output signal from a node connecting the third and fourth transistors. A differential amplification circuit functions in accordance with the first and second output signals. The first and fourth MOS transistors each have a gate for receiving a first input signal. The second and third MOS transistors each have a gate for receiving a second input signal having a phase inverted from the phase of the first input signal.